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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/636,591	08/10/2000	Shuhei Kato	P100341-00003	6504

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EXAMINER	
LAO, LUN S	

ART UNIT	PAPER NUMBER
2614	

NOTIFICATION DATE	DELIVERY MODE
10/22/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/636,591	KATO ET AL.	
	Examiner	Art Unit	
	LUN-SEE LAO	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4 and 5* is/are allowed.

6)☒ Claim(s) *2,3 and 6-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This action responds to the amendment filed on 08-04-2008. Claim 3 has been amended and claim 1 has been canceled. Claims 2-14 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-3 and 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malcolm (US Pat. 6,373,954) in view of Tsukamoto et al. (US PAT. 4,815,352) and Inoue et al. (US PAT. 5,532,765).

Consider claim 3, Malcolm teaches a sound processor formed on a single semiconductor device to reproduce pulse-code-modulated sound waveform data, comprising (see abstract):

sequence control means (see fig.1A, 121, 122,120, such as first in, first out and see col. 11 line 57-62);

bus interface means (101) for a common bus including an address bus and a data bus;

bus master means (103) for issuing an address to said common bus through said bus

interface means (101) under control of said sequence control means (103), and reading and writing data for a resource connected to said common bus; data holding means (103) for holding part of data read out by said bus master means (103); M sets (M being a natural number) of independent digital/analog converting means ((110) for converting digital data over a sound channel into an analog sound signal;

data output control means (118, DSP) for controlling an output of data to said digital/analog converting means (110 and see col. 10 line 28-col.11 line 62); but Malcolm does not clearly teach that time division multiplexing means for time-division-multiplexing and outputting data of over N sets (N being a natural number greater than 2) of sound channels to each of digital/analog converting means required for reproduction; whereby data is to be simultaneously reproduced over a plurality of sets of sound channels represented by a product of M and N, wherein said digital/analog converting means is structured by a plurality of digital/analog converters and said digital/analog converters are in cascade connection, said cascade connection being a connection that an output of each of said digital/analog converters is connected to another one of said digital/analog converters as a reference voltage.

However, Tsukamoto teaches that time division multiplexing means (see fig.17, 6-7) for time-division-multiplexing and outputting data of over N sets (N being a natural number greater than 2) of sound channels to each of digital/analog converting means (91-93) required for reproduction (see abstract andcol.8 lines 15-55); whereby data is inherently to be simultaneously reproduced over a plurality of sets of sound channels represented by a product of M and N (see fig.17 and col.16 line 20-62).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Tsukamoto in to Malcolm so that a plurality of the wave data are provided in a time division multiplex form from said wave memory through the time division multiplex calculation by said address calculator for the wave memory to improve the sound quality.

On the other hand, Inoue teaches that said digital/analog converting means is structured by a plurality of digital/analog converters and said digital/analog converters are in cascade connection, said cascade connection being a connection that an output of each of said digital/analog converters is inherently (because, when a bit date output from D/A((28) in fig.19) transmitting into the D/A ((29) in fug. 19) which is including a reference voltage, and the output of the D/A is connected to the input of the succeeding D/A ; (see fig.19, 28-39) (see col. 14 line 34-63)) connected to another one of said digital/analog converters as a reference voltage (see fig.19 (28-39) and col. 14 line 22-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Inoue in to Malcolm to prevent the signal energy to drop quickly.

Consider claim 2, Malcolm teaches a sound processor of bus master means (see fig.1A, 103) further has a function of determining whether data required in reproduction is stored in said data holding means or not, and acquiring the data from a resource connected to said common bus and storing the data in said data holding means (103)

where the data required in reproduction is not stored in said data holding means (103 and see col10 line 28-58).

Consider claim 8-9, Tsukamoto teaches a sound processor of the data output means (see fig. 17) further has a function of outputting data in later timing, with respect to timing (6,7) of outputting data to a certain digital/analog converter (91-93), to a digital/analog converter connected in a next stage thereto, and controlling timing (by microcomputer) of outputs to eliminate interference between time slots due to signal delay between said cascade-connected digital/analog converters (91-93) when outputting data to said cascade-connected digital/analog converter (91-93 and see col.16 line 20-col.16 line 61) and a sound processor of the data output control means (microcomputer) is to be programmably set in timing of outputting data (see col. 16 line 20-col.17 line 61).

Consider claim 10-12, Malcolm teaches a sound processor of the sound waveform data is configured by two arrays (array 0 and array 1 and see table 67) having end codes provided at respective terminal ends of the arrays (see col.120 line 35-col.121 line 62), and said bus master means (see fig.1A, 103) further having a function to start reading at a head of the first array (array0), uninterruptedly starting reading at a head of the second array (array1) immediately after reading the end code of the first array (array0), and uninterruptedly starting reading at the head of the second array (array1) after reading out the end code of the second array (arry1 and see col.119 line 19 –col. 122 line 63); and a sound processor of further comprising accumulating means (see fig.3, 315) and means (see fig. 45) for storing pitch control information (by

microcontroller), wherein the pitch control information is read out at a constant time interval (see col.119 line 19-67) and accumulated by said accumulating means (see fig.3, 315), and one part or the whole of an accumulation result being utilized as address information for access to a common bus of said bus master means (see fig.1A,103 and col.12 line 41-col.13 line 26); and a sound processor of the bus interface means (see fig.1, 101) is provided independent for a plurality of common buses.

Consider claim 13, Malcolm teaches a sound processor of further comprising interrupt request control means (see fig.1, 103 and col. 38 line 42-67) to be controlled by said sequence control means(see fig.1 121, 122,120, such as first in, first out and see col. 11 line 57-62); and generate an interrupt request signal, wherein said bus master means (see fig.1A, 103) comprises waveform reading control means (see fig. 43L, 430 and col. 108 line 60-col.111 line 67) to control reading of sound waveform data, envelope/preset control means (see fig.1, 103) to control reading out of parameters for controlling envelope data and sound reproduction (see col. 119 line 19-67), and access arbitrating means (microcontroller and software) an to arbitrate between an access of from said envelope/preset control means to the common bus and an access of from said waveform reading control means (microcontroller) to the common bus (see col. 99 line 7-51 and col.119 line 19-col.120 line 67), said bus interface means (see fig.1A, 101) comprising first bus interface means (101) to a first common bus, and second bus interface (109) to a second common bus (see col.10 line 20-64).

Consider claim 14, Malcolm teaches a sound processor apparatus, comprising:

being configured on one single semiconductor device (see abstract), first and second buses (see fig.1, 101,105) having independent data transfer capabilities,

a central processing unit (see fig1, 103 microcontroller) and a sound processor (118, DSP) according (see col.10 line 28-64) to claim 12 or 13 (see previous rejection claim 1 and claim 12 or 13) as bus masters (see fig.1, 101) for said first and second buses, a memory connected to said first bus, a first bus arbitrating means (see fig.1A, 101) to administer arbitration over said first bus (see col. 10 line 28-65), and a second bus arbitrating means (109) to administer arbitration over said second bus (109, and see col.10 line 50-65).

4. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malcolm (US Pat. 6,373,954) as modified by Tsukamoto et al.(US PAT. 4,815,352) and Inoue et al. (US PAT. 5,532,765) as applied to claim 1 above, and further in view of Anderson (US PAT. 6,078,594).

Consider claim 6, Malcolm and Tsukamoto, Inoue do not clearly teach a sound processor of the data output control means further has a function to control a çonstant period of a mute state between adjacent sound channels time-division-multiplexed.

However, Anderson teaches a sound processor of the data output control means further has a function to control a constant period of a mute state between adjacent sound channels time-division-multiplexed (see col.11 lines 35-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Anderson into the teaching of

Malcolm and Tsukamoto, Inoue to provide to the latency of channel changes through the use of flags that are passed with the data between the transport demultiplexor and decoder.

Consider claim 7, Anderson teaches a sound processor of the mute state has a period to be set programmable (see col.6 line 27-51).

Allowable Subject Matter

5. Claims 4-5 are allowed.

Response to Arguments

6. Applicant's arguments filed 08-04-2008 have been fully considered but they are not persuasive.

Applicant argued that "by the claimed invention, if the D/A converters are cascade-connected to each other, it is possible to reduce the number of bits of each converter, and thus, to greatly reduce the area needed for the D/A converter. For example, by the claimed invention, if a 16-bit D/A converter is required, two 8-bit D/A converters may be cascade-connected to construct the 16-bit converter. In such a case, the area for the 8-bit D/A converter becomes 1/256 of the area for the 16-bit D/A converter, and therefore, even if two 8-bit converters are needed, the area is 2/256 of the 16-bit converter" (see the remarks page 12 second paragraph).

The examiner responds the argument "the D/A converters are cascade-connected to each other, it is possible to reduce the number of bits of each converter, and thus, to greatly reduce the area needed for the D/A converter" is not claimed, and thus moot.

Applicant further argued that " the description of Inoue that these D/As 28-39 are not cascade-connected" (see the remarks page 13, 3rd paragraph).

The examiner disagrees with that. Inoue disclose that said digital/analog converting means is structured by a plurality of digital/analog converters and said digital/analog converters are in cascade connection (see fig. 19 (28-39)), said cascade connection being a connection that an output of each of said digital/analog converters is inherently (because, when a bit date output from D/A(28, in fig.19) transmitting into the D/A (29, in fig. 19) which is including a reference voltage for transmitting the bits, and the output of the D/A is connected to the input of the succeeding D/A ; (see fig.19, 28-39) (see col. 14 line 34-63)) connected to another one of said digital/analog converters as a reference voltage (see fig.19 (28-39) and col. 14 line 22-67). Therefore, the combination meets the limitation as recited in the claim 3.

Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any response to this action should be mailed to:

Mail Stop ____(explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Facsimile responses should be faxed to:
(703) 872-9306

Hand-delivered responses should be brought to:
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lao,Lun-See whose telephone number is (571) 272-7501 The examiner can normally be reached on Monday-Friday from 8:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin, can be reached on (571) 272-7848.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 whose telephone number is (571) 272-2600.

Lao,Lun-See
/Lun-See Lao/
Examiner, Art Unit 2615
Patent Examiner
US Patent and Trademark Office
Knox
571-272-7501
10-17-2008

/Vivian Chin/
Supervisory Patent Examiner, Art Unit 2614